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The feasibility of the heteroepitaxy of high quality GaAs on SOI substrates by the OMCVD process was investigated. The motivation for this is the potential to obtain large area GaAs wafers with improved radiation hardness and, eventually, the monolithic integration of radiation hardened Si and GaAs components. Epitaxial GaAs has been grown on SOI wafers prepared by both isolated silicon epitaxy (ISE) and high-dose oxygen implantation (SIMOX). The use of SIMOX provided an efficient means to obtain SOI wafers with the proper Si surface orientation compatible with a standard GaAs on Si growth technology and an excellent surface morphology was achieved. An optimally oriented ISE surface was appparently not obtained with the resulting surface morphology typical of growth on a singular (100) surface. However, the GaAs grown on ISE shows an improved defect structure while the

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Epitaxial GaAs on SOI Wafers

Final Report

Dr. J. P. Salerno

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Abstract

The feasibility of the heteroepitaxy of high quality GaAs on SOI substrates by the OMCVD process was investigated. The motivation for this is the potential to obtain large area GaAs wafers with improved radiation hardness and, eventually, the monolithic integration of radiation hardened Si and GaAs components. Epitaxial GaAs has been grown on SOI wafers prepared by both isolated silicon epitaxy (ISE) and high-dose oxygen implantation (SIMOX). The use of SIMOX provided an efficient means to obtain SOI wafers with the proper Si surface orientation compatible with a standard GaAs on Si growth technology and an excellent surface morphology was achieved. An optimally oriented ISE surface was apparently not obtained with the resulting surface morphology typical of growth on a singular (100) surface. However, the GaAs grown on ISE shows an improved defect structure while the high quality oxide/silicon interface characteristic of the ISE process is maintained. A n-channel GaAs on SOI FET profile was achieved by doping during the epitaxy process. The C-V doping profile of this structure showed flat doping plateaus for both the channel and contact levels, excellent abruptness, and a residual carrier concentration of less than 10^{14} cm^{-3}. Complete isolation was achieved for discrete FETs fabricated at Kopin on GaAs on SOI by etching to the buried oxide layer. The FETs showed good performance with a measured transconductance of 68 mS/mm for a 3 micron gate length device with a 9 micron source-drain spacing. The observed complete isolation provides a major advantage for elimination of back and side gating effects frequently observed in FETs fabricated in bulk GaAs wafers.

1.0 Introduction

Technologies for the fabrication of both GaAs on Si and silicon on insulator (SOI) wafers have seen exceptional advancement over the last several years. The GaAs on Si technologies offer the opportunity to obtain epitaxial electronic and optoelectronic III-V components on large-area low-cost wafers. The development of SOI wafers is directed toward the achievement of radiation hardened Si devices as well reducing process complexity and cost while improving the performance of VLSI circuitry. The combination of these two technologies offer significant opportunities for both military and commercial electronics. These GaAs on SOI wafers could improve the radiation hardness of GaAs devices due to the presence of the insulating buried oxide. Processing techniques for GaAs could also be modified to achieve true dielectric isolation via the buried oxide. This could prove to be a viable approach for the elimination of backgating effects and thus enable the fabrication of more complex GaAs digital circuits. Development of this materials technology could also lead to the monolithic integration of radiation hard SOI components with GaAs electronics and optoelectronics.

This research program has been directed toward the demonstration of the growth of high quality GaAs epitaxial layers on SOI substrates. For the scope of this program, the SOI terminology denotes wafer for which a Si layer is isolated by an insulator from a Si substrate. This type of technology, which excludes silicon-on-sapphire (SOS), is the most viable for current and future applications, because of material quality, cost, and manufacturing considerations. During this program Kopin has successfully applied its WAFER ENGINEERING technology to the growth of GaAs on SOI and achieved epitaxial GaAs layers having surface quality, uniformity, and defect densities comparable to that seen for direct growth of GaAs on bulk silicon substrates. The use of SOI substrates for which the Si layer surface has a slight intentional misorientation from the (100) was found to suppress the formation of antiphase defects that has been observed in all previously reported GaAs on SOI investigations [1-3]. Additionally, epitaxial FET structures were grown, electrically profiled, and devices successfully fabricated and tested. The epitaxial buffer layer shows good depletion through the buffer layer and the fabricated transistors show performance comparable to their GaAs on Si counterparts. Complete electrical isolation of these transistors was demonstrated by etching down to the buried oxide surface, illustrating the basic concept of GaAs on Insulator properties.

Both Isolated Silicon Epitaxy (ISE) and high-dose oxygen implanted (SIMOX) SOI wafers were used as substrates for this investigation. These two processes are currently regarded as the most viable approaches for commercial applications of SOI. While

the ISE process appears to be the higher quality and lower cost approach, the use of the SIMOX wafer is particularly relevant to this Phase I feasibility investigation. The reason for this is that by forming a buried oxide through implantation, the misorientation of the bulk Si substrates used for Kopin's standard GaAs on Si process could be maintained. In this fashion we were able to quickly demonstrate that SOI wafers could be used as substrates for GaAs heteroepitaxy without the formation of antiphase boundaries. Epitaxial GaAs was successfully grown on both types of SOI substrates investigated. There are several potential advantages associated with the use of ISE substrates including greater flexibility of Si and oxide layer thicknesses, lower cost, and a higher quality Si layer which will be of significance for the eventual monolithic fabrication of both Si and GaAs devices on a single GaAs on SOI wafer. Additionally, our preliminary analysis of the defect structure indicates that the residual threading dislocation are confined closer to the GaAs/Si interface for growth on ISE wafers than they are for growth on SIMOX wafers.

The remainder of this final project report consists of sections discussing the background for this work, the scope of the work performed described by task, a presentation and discussion of the research results, a section identifying and discussing critical issues to be considered in a Phase II program, and a summary.

1.1 Background

Development of epitaxial III-V materials on Si substrates has progressed rapidly during recent years. In particular, the use of GaAs on Si wafers offer several opportunities for electronic and optoelectronic device and integrated circuit fabrication. These include larger wafer diameter, improved wafer mechanical properties, higher wafer thermal conductivity, and the ability to monolithically integrate Si circuitry with GaAs electronic and optoelectronic devices and circuits. These wafers allow the combination of the cost effectiveness and quality of Si wafers with the performance and radiation hardness of advanced AlGaAs/GaAs heterostructure devices. The technology is not limited to only GaAs as other III-V materials have grown on Si substrates.

Advances in the technology for lattice mismatched heteroepitaxy of GaAs on Si substrates over the last several years have generated great interest in this engineered material structure. Various methods have been utilized to obtain reasonably high quality GaAs on Si epitaxial layers. These include vapor phase epitaxy (VPE) on Ge-coated Si substrates [4] as well as direct growth on Si substrates by molecular beam epitaxy (MBE) [5] and organometallic chemical vapor deposition (OMCVD) [6]. The quality of GaAs on Si wafers has advanced to

the point where GaAs ring oscillators [7], 1K static RAMs [8], and monolithic integration of GaAs LEDs and Si MOSFETs [9] and GaAs MESFETs and Si CMOS circuits [10] have been demonstrated. Growth of GaAs on silicon-on-sapphire (SOS) has also been achieved and FETs demonstrated in this material [11].

Research and development at Kopin over the past three years has led to significant technology demonstrations relevant to the commercialization of GaAs on Si technology, including the demonstration of uniform and high quality GaAs on Si on 4" and 6" diameter substrates [12,13], high reliability digital circuits fabricated using a commercial foundry process [14], and both 0.8 [15] and 1.3 [16] micron emission wavelength laser diodes. These results are discussed here in order to point out that Kopin's standard GaAs on Si process provides heteroepitaxial wafers that are among the highest quality achieved worldwide. Our intention for this program was to leverage on this existing technology in order to assess the feasibility to grow high quality GaAs on SOI substrates.

Kopin prepares heteroeptiaxial GaAs on Si wafers through the use of a manufacturable two-step organometallic chemical vapor deposition (OMCVD) process for which trimethylgallium and AsH_3 are the source materials. Using a combination of thermal processes, we have been able to reduce the defect densities in these layers to the 10^6 to 10^7 cm^{-2} range, as evidenced by x-ray rocking curve linewidth measurements and transmission electron microscopy [12,13]. Additionally, we have achieved surface properties suitable for lithographic fabrication of submicron features. These surfaces show rms surface roughness of approximately 2 nm, comparable to polished GaAs wafers, as measured with a surface profilometer. Using these materials we have fabricated epitaxial GaAs MESFETs with transconductance greater than 100 mS/mm for 1 um gate lengths [17].

In parallel with GaAs on Si technology, silicon on insulator technology has been intensively developed since it offers improved circuit performance compared to bulk Si circuits. This results from the complete dielectric isolation of the devices. The SOI circuits offer higher packing density, higher radiation tolerance, faster switching speeds, and CMOS designs that are free of latch-up. Several approaches to obtain SOI materials have been studied. The two most promising ones are ISE and SIMOX. In the ISE process, of polycrystalline Si deposited on oxidized Si wafers is recrystallized by using a graphite strip heater [18]. The ISE SOI material has been demonstrated to be device worthy through the successful fabrication of devices as complex as 16K SRAMs containing $1.2x10^5$ transistor arrays [19].

Kopin has developed a ISE system for the production of SOI wafers up to six inches in diameter. Using this system SOI wafers have been fabricated with defect densities as low as 10^5 cm^{-2} and

minority carrier lifetimes up to 30 microseconds [20]. These ISE wafers are free of sub-boundaries and have excellent crystalline quality. In the ISE process, Si wafers are first oxidized to form an insulating oxide between 0.75 and 3 microns. Polycrystalline Si is then deposited to a thickness ranging from 0.3 to 5 um. This structure is capped with an oxide layer. In the ISE system, this wafer is heated on a platen to approximately 1100 C and a narrow strip heater is scanned above the surface to melt the polycrystalline Si layer. This layer recrystallizes to form the SOI wafer. By seeding the recrystallization through a small area contact to the supporting Si substrate a single crystal layer can be obtained [21].

The SIMOX process was used to form a buried oxide in Si wafers misoriented 3 degrees from the (100) toward the (111). In this process, oxygen ions are implanted at high energy so they penetrate far below the wafer surface and with a large range distribution. A very high dose is used so as to affect a compositional change. A high temperature anneal following the implant results in the formation of a buried SiO_2 layer. Some limitations of this technique are the inherently thin oxide, poorer abruptness of the silicon/oxide interfaces, and low wafer throughput.

In addition to the commercialization cost advantages for large-area wafers, the most attractive attributes of ISE SOI for GOS on SOI growth is the low defect density and the purity of the Si layer achieved by this process in comparison to either conventional SOS or SIMOX material. This should lead to better Si device performance, lower defect densities in the GaAs layer, and, hence, better GaAs device performance. Additionally, high defect densities in the Si layer can interfere with the heterogeneous nucleation and growth of the GaAs layer. The defects can act as preferential nucleation sites and can cause faceting of the surface of the growing film. They can also act as diffusion pipelines with the effect of autodoping the growing GaAs layer. These effects may be the cause of the poor surfaces previously achieved for GaAs grown on SIMOX wafers [1-3].

The exact (100) orientation of typical ISE SOI films, however, may pose some problems for GOS growth. Although the preferred wafer orientation of GaAs device fabrication is the (100), in order to achieve high quality epitaxial GaAs on Si it is desirable to use a Si substrate slightly misoriented from the (100) in any direction except towards the nearest (110). If this is not done, antiphase domains can form in the epitaxial layer due the polar nature of GaAs. Experience indicates that misorienting the Si by 2 to 6 degrees off the (100) toward the (111) gives the highest quality GaAs. There have been recent reports by Japanese researchers, however, that high quality GaAs can be achieved for growth on the exact (100) Si surface. There is speculation that single domain growth on the exact (100) is

dependent on the pre-growth treatment of the Si surface, and the resulting reconstruction of the atomic arrangement at the surface, prior to nucleation of the GaAs. Therefore, in order to take full advantage of the benefits of GaAs on ISE SOI, it is appropriate to investigate to what extent control of the surface orientation of the SOI film is required.

1.2 Approach

The approach taken during this research activity consists of five tasks as listed in Table 1. The tasks were focused towards feasibility assessment and directed to the project goal of determining epitaxial GaAs could be grown on a SOI substrate with comparable quality to that grown on a bulk Si substrate.

Table 1
Accomplished Phase I Program Tasks

	Task	Objectives
1	SOI Substrate Experiments	To determine the feasibility of obtaining SOI wafers misoriented off the (100).
2	OMCVD growth of GaAs on SOI wafers	Apply GaAs on Si nucleation, growth, and defect reduction techniques to GaAs on SOI growth.
3	Characterization	To determine the properties of GaAs on SOI wafers in comparison with GaAs on Si wafers.
4	FET fabrication and testing	To assess the quality of the GaAs on SOI materials with respect to majority carrier transport and device process compatibility.
5	Identification of problem areas	To make an overall assessment of the project feasibility and to formulate the Phase II research plan.

The first task to be addressed was the feasibility to generate an SOI wafer where the Si layer on the oxide is sufficiently and correctly oriented so as to suppress the

formation of antiphase domains. For this activity, several ISE runs were made for which the starting substrate was misoriented from the (100) so as to permit the growth of high quality GaAs on Si. The recrystallization of the polysilicon layer during the ISE process was seeded from this layer. In addition, SIMOX substrates were obtained from a commercial source for which the implantation was done directly into Si wafers, provided by Kopin, with the correct orientation for GaAs on Si growth. This approach was deemed the most rapid and reliable for achieving the demonstration goals of this project.

The second task encompassed the actual growth of GaAs on the SOI substrates by OMCVD. For this activity Kopin employed its standard techniques for wafer cleaning and pregrowth treatment, heterogeneous nucleation and growth initiation, and defect reduction. For this program, similar structures were grown on ISE SOI, SIMOX SOI, and bulk Si substrates. This permitted comparison of the properties of the epitaxial GaAs for each of the substrate materials. Both seeded and unseeded ISE SOI wafers were used.

Both the third and fourth tasks were focused on assessment of the properties and quality of the GaAs on SOI wafers. The third task was concerned directly with materials evaluation. Factors considered were epitaxial layer surface quality, wafer flatness, crystalline quality, and achievable doping profiles and buffer layer depletion. The fourth task focused on evaluation of the the wafer properties from the standpoint of both the fabrication and operation of GaAs majority carrier devices. Standard lithographic, metallization, and etching techniques were employed for the fabrication of GaAs FETs for which the active device layers were grown as part of the GaAs on SOI heteroepitaxy process. The transistor characteristics, including isolation via the buried oxide, were measured.

The fifth task dealt with the identification and assessment of problem areas that need to be considered in generating a Phase II proposal. The problems noted need to be either explored or avoided during a Phase II program.

The results of each of these tasks are presented and discussed in the next section of this report.

2.0 Results and Discussion

The section presents a discussion of the experimental techniques and results obtained for this research program. The subsequent sections are divided to correspond with the tasks discussed in section 1.2.

2.1 SOI Substrate Experiments

The purpose of this task was to determine if the Si layer of an SOI wafer could be formed so as to constrain the surface to the preferred orientation for GaAs on Si epitaxy. This was investigated for both the ISE and SIMOX processes. The basis for these experiments was to conduct the SOI processes on wafers having the surface orientation used in our standard process for heteroepitaxy of GaAs on bulk Si. The starting Si wafers for this investigation were misoriented 3 degrees from the (100) toward a {111} plane. Misorientation of the Si wafer in this direction is known to suppress the formation of antiphase domains and wafers of this type have been used for demonstration of the growth of high quality GaAs on Si wafers as large as six-inches in diameter [13].

The SOI wafers were formed by the ISE process as follows. The starting wafers were cleaned and then thermally oxidized to form a 1 micron thick SiO_2 layer. For some of the wafers an opening was made in the oxide to permit seeding from the substrate. A 1 micron thick polysilicon layer was then deposited and this was followed by the deposition of a protective oxide layer. These wafers were run through Kopin's standard ISE process in which a movable heater is passed slowly across the wafer surface to locally melt the polysilicon layer. The subsequent recrystallization results in a 1 micron thick single crystal layer of Si on the thermal oxide surface.

The SIMOX wafers were prepared by ion implantation of O^+ into three-inch diameter 50 ohm-cm boron doped Si wafers. The oxygen ion dose was 1.8×10^{18} cm^{-2} at a voltage of 200 KeV and a beam current of 37 mA. The implant was done with a wafer temperature of 600 °C. Following the implant, the wafers were annealed at 1300 °C for 6 hours. The implantation and a post implant anneal were performed at IBIS Corporation, Beverly, MA. Optical characterization of the SIMOX wafers showed the respective thicknesses of the buried oxide and Si layers to average 0.3 and 0.24 microns.

The aim of this task was to determine if an SOI wafer could be obtained with the Si layer having the preferred orientation for suppression of antiphase domains in GaAs on Si growth. Additionally, it is preferred in general that substrates used for OMCVD be slightly off a singular surface orientation. This aids in achieving good surface morphology and adds a greater degree of control to the epitaxy process. Laue x-ray diffraction experiments were used for this investigation and both the SIMOX and ISE wafers showed diffraction patterns equivalent to the starting substrate orientation. However, this data may be misleading in that the presence of the substrate might dominate the diffraction because the Si layers are so thin and further investigations are needed.

2.2 OMCVD of GaAs on SOI Substrates

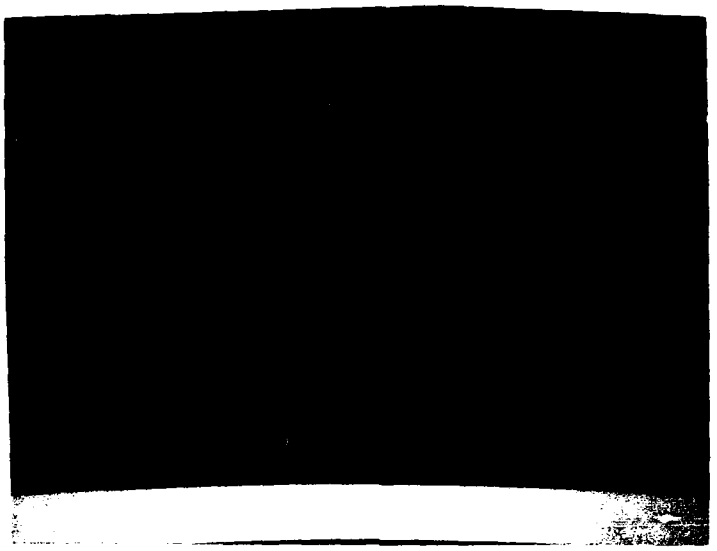
The purpose of this task was to employ OMCVD heteroepitaxy techniques previously developed at Kopin for the growth of GaAs on SOI substrates. For this task, OMCVD was employed using trimethylgallium and arsine as the primary source chemistry. This was supplemented by the use of Si as an n-type dopant for the growth of epitaxial FET structures for characterization purposes. For this project epitaxial GaAs was grown on both seeded and unseeded ISE SOI wafers and on Si wafers in which a buried oxide was formed by ion implantation (SIMOX). The data is compared to that representative of the experience with growth of GaAs on bulk Si substrates.

The substrate wafers were prepared as discussed in section 2.1 above. The ISE wafers surfaces were typical of Kopin's standard process. The surfaces of the as-received SIMOX wafers were found to be textured when examined by Nomarski contrast optical microscopy.

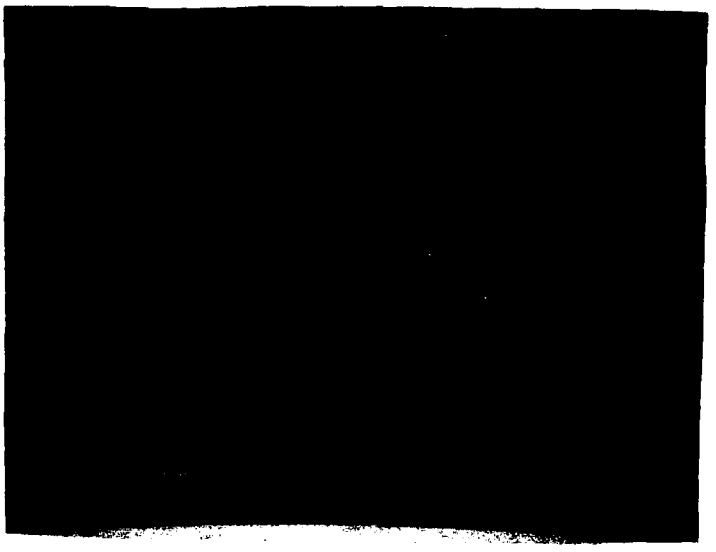
The GaAs heteroepitaxy was done using a two-step growth technique. A low temperature nucleation step (~450 °C) provides a continuous layer for subsequent two-dimensional epitaxial growth. The GaAs layers were grown at 650 °C and consisted of a 2.5 micron buffer layer followed by a 0.15 micron layer doped at $n=1x10^{17}$ cm^{-3} and a 0.1 micron layer doped at $n=1.8x10^{17}$ cm^{-3}. These two doped layers serve as the channel and contact layers for FETs and aid in assessing the electrical properties of the epilayer via C-V dopant profiling.

Analysis of the surface morphology of the GaAs epitaxial layers grown on both the seeded and unseeded ISE wafers revealed a rough surface characteristic of epitaxy on the (100) by OMCVD and also suggested the presence of antiphase domains. This indicates that the Si layers formed by the ISE process have (100) surface orientations and that seeding from the 3° misoriented Si wafer had limited influence on the recrystallized layer orientation. Excellent surface morphology was obtained for the GaAs layers grown on oxygen implanted SOI wafers. In addition, the haze of the GaAs layer grown on the SIMOX wafers is much less than that of the starting SOI wafer, as indicated by a comparison of Figures 1 (a) and (b). The haze was reduced from a typical value of 10000 for the starting SIMOX surfaces to less than 1000 for the GaAs epilayer grown on the SIMOX substrate. This number is a measure of the amount of light scattered out of an incident laser beam by the surface features, with a lower number corresponding to a smoother surface.

Figures 2 and 3 compare Nomarski contrast optical micrographs of GaAs epilayers grown on ISE and SIMOX substrates.



(a)

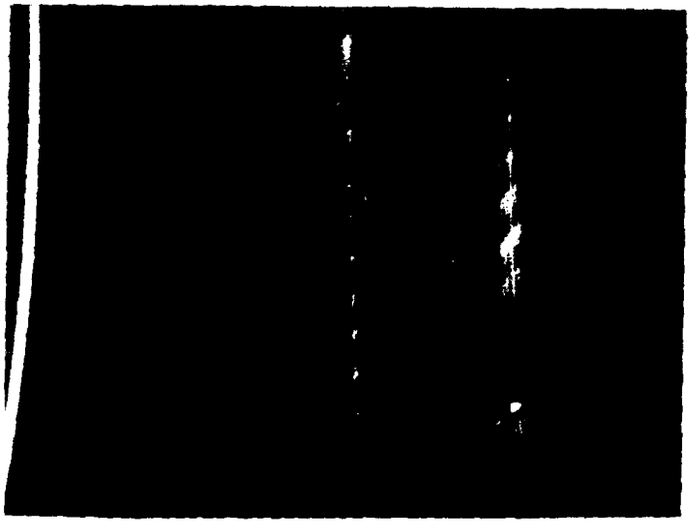


(b)

Figure 1: Surface haze maps of (a) an as received implanted oxide SOI wafer and (b) a 2.5 micron heteroepitaxial GaAs layer grown on this wafer.

Simox

250μm



ISE

Figure 2: Low magnification Nomarski contrast optical micrographs comparing surface morphologies of heteroepitaxial GaAs on SIMOX and ISE wafers.

Simox

25μm

ISE

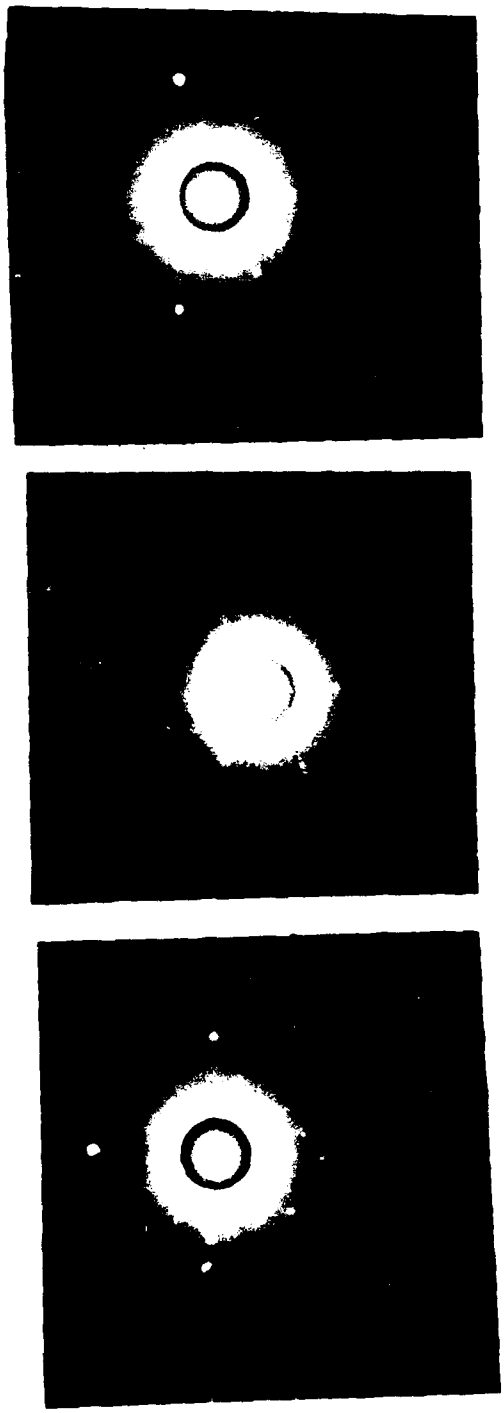
Figure 3: High magnification Nomarski contrast optical micrographs comparing surface morphologies of heteroepitaxial GaAs on SIMOX and ISE wafers.

The low magnification micrographs in Figure 2 show the epitaxial layer grown on SIMOX to be essentially featureless while the layer grown on the ISE wafer shows linear features. This type of surface morphology is also obtained for Si epitaxy on some ISE wafers and is currently under investigation. However, there are areas of the surface that show excellent surface morphology. This local morphology, which is better than that obtained for GaAs on SIMOX and among the best ever obtained for GaAs on Si heteroepitaxy, is shown in the higher magnification micrographs in Figure 3. Note the area of clean morphology in the GaAs on ISE wafer. While over only a small area, it represents an excellent GaAs on Si morphology. The crystallography associated with the development of such an excellent morphology may be investigated in the Phase II proposal. The irregular features observed in this micrograph can be attributed to growth on a singular (100) surface where both defect delineation and antiphase domain formation may occur. Note that the corresponding micrograph of the GaAs on SIMOX wafer show it to be free of such features. This indicates that the SIMOX layer surface has the orientation of the starting Si wafer.

Figure 4 shows Laue x-ray diffraction patterns obtained from (a) a 3° misoriented bulk Si wafer typical of those used as starting materials in these experiments, (b) an epitaxial GaAs layer grown on a SIMOX substrate, and (c) an epitaxial layer grown on a ISE substrate. Note that the GaAs on SIMOX diffraction pattern is identical in orientation to the pattern obtained from the Si wafer except that certain reflections are accentuated due to the structure factor for GaAs. However, there are two patterns obtained from the GaAs on ISE wafer; one associated with the misoriented substrate and a second oriented exactly on the (100) and with reflection intensities characteristic of GaAs. Thus it is concluded that the GaAs on ISE wafer characteristics result from growth on an exact (100) Si surface.

All these data support the conclusion that the ISE Si layer did not take the orientation of the seed substrate. This explains the observed surface morphology. However, even in this case the growth was epitaxial and local regions display excellent surface quality.. This observation should be explored further in a Phase II activity.

Growth on the oxygen implanted SOI wafer proved extremely successful. The obtained morphology indicates that the use of a misoriented substrate as the host for the buried oxide successfully avoided the formation of antiphase domains previously encountered in most previously published work [1-3]. The surface morphology was comparable to that typically obtained for growth on GaAs directly on bulk Si wafers. As will be seen in the next sections, the electrical, structural, and device properties of these wafers is also comparable to GaAs on bulk Si.



(a)

(b)

(c)

Figure 4: Laue x-ray diffraction patterns obtained from (a) a 3° misoriented bulk Si wafer typical of those used as starting materials in these experiments, (b) an epitaxial GaAs layer grown on a SIMOX substrate, and (c) an epitaxial layer grown on an ISE substrate.

2.3 Materials Evaluation

Further materials evaluation performed on the GaAs on SOI wafers included wafer flatness, double crystal x-ray rocking curve measurements, transmission electron microscopy, and C-V doping profiling. The flatness measurements were done both before and after GaAs growth for the 3" diameter SIMOX wafers. Table 2 shows the flatness data for the as received wafers. The measurements are done with a contactless capacitance technique. The table lists values for total thickness variation (TTV), focal plane deviation (FPD), total indicated reading (TIR), and warp. The units of measurement for all these parameters are microns and it is desirable to have these values as close to zero as possible. Any influence of the buried oxide layer on this measurement is not known. The flatness parameters were again measured after growth of 2.5 microns of GaAs on wafers 1 and 5. The measured values are shown in Table 3.

Table 2
Flatness Data for As-Received SIMOX Wafers
(all data is in microns)

Wafer#	TTV	FPD	TIR	Warp
1	17.9	10.7	18.7	36.0
2	15.3	13.7	22.4	19.4
3	15.4	13.5	20.8	12.1
4	15.1	13.2	21.4	12.2
5	18.2	20.5	32.6	15.2

Table 3
Flatness Data for GaAs on SIMOX Wafers
(all data is in microns)

Wafer#	TTV	FPD	TIR	Warp
1	1.8	-0.5	0.8	50.5
5	3.5	-0.7	1.2	22.0

Note that the values of TIR, TTV, and FPD are reduced after the GaAs growth. This trend is very encouraging although the buried oxide layer might influence the data and further investigation is required. The warp is only observed to increase by a few microns

and at these values should not have significant influence on device processing. These values for TIR, TTV, and FPD are well within the standard specification range for bulk GaAs wafers. The warp is similar to that of GaAs on Si wafers and does not affect standard wafer processing.

Double crystal x-ray rocking curve data was taken for these samples. The data showed peak widths (FWHM) of approximately 200 arc seconds. This is only slightly above the 180 arcseconds typically observed for similar thickness layers of GaAs grown on bulk Si substrates. The structural quality of the GaAs epilayers was further investigated by cross sectional TEM. Figures 5 and 6 show cross sectional TEM micrographs of GaAs on SIMOX and ISE substrates, respectively. For scaling purposes, recall that the Si layer thicknesses are 0.25 for SIMOX and 1 micron for ISE. The thin dark region observed in the Si layer in Figure 6 may be an artifact of the TEM sample preparation. These data show several interesting features:

1. There are no nucleation-induced stacking faults in either wafers, dislocations being the only type of defect observed. This is consistent with good GaAs epitaxy on bulk Si wafers.

2. The dislocations are confined to a region much closer to the GaAs/Si interface for the GaAs on ISE wafer than the GaAs on SIMOX wafer. Furthermore, preliminary indications are that the dislocations in the two wafers have different characteristics.

3. Some defects exist in the GaAs on ISE wafer, which may be attributable to antiphase domains, but at a much lower level that expected given the apparent (100) orientation of the layer.

These results clearly demonstrate the feasibility to grow GaAs of high crystallographic quality, comparable to that grown on bulk Si substrates. Thus the overall objective of the Phase I research program has been satisfied.

The ability to controllably dope the GaAs epilayer is critical for device applications. We have successfully grown an epitaxial FET structure using silicon as the n-type dopant. This structure consisted of a 2.5 micron thick nominally undoped buffer followed by a 0.15 micron channel layer doped at $n=1x10^{17}$ cm^{-3} and a 0.1 micron thick contact layer doped at $n\sim2x10^{18}$ cm^{-3}. This doping profile of this structure was measured after growth using an electrochemical C-V profile. The profile, shown in Figure 7, exhibits flat doping plateaus and characteristically abrupt transitions. The residual buffer layer carrier concentration is observed to be below 10^{14} cm^{-3}.

Figure 5: Cross sectional TEM micrograph of GaAs on SIMOX wafer.

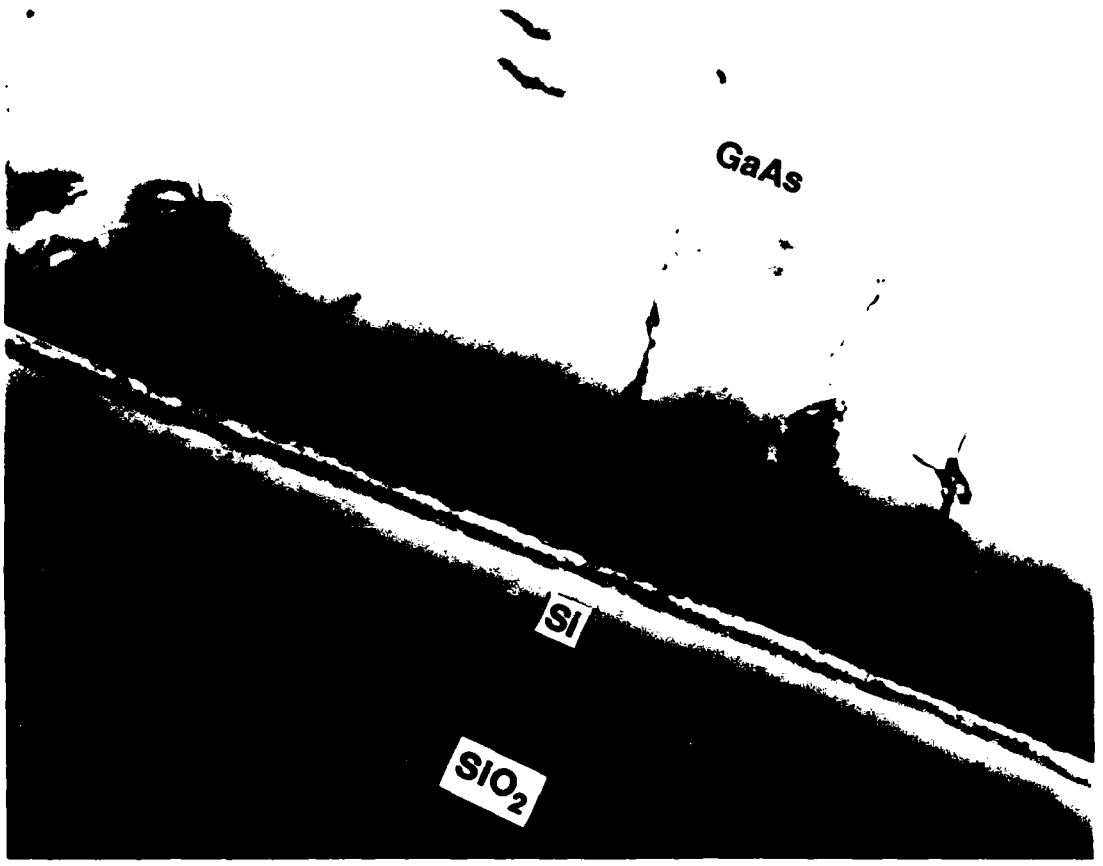


Figure 6: Cross sectional TEM micrograph of GaAs on ISE wafer.

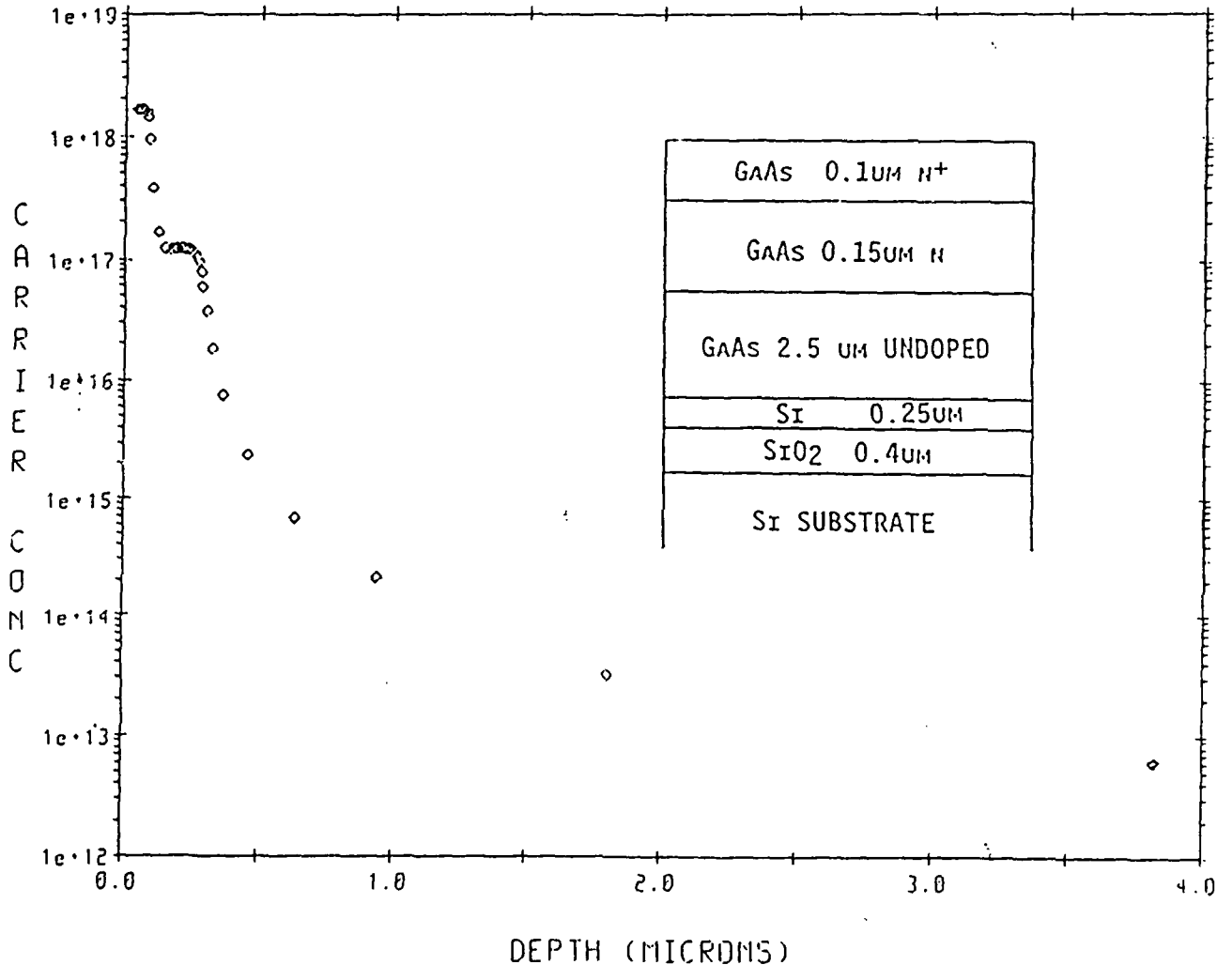


Figure 7: Doping profile for epitaxial GaAs FET structure grown on a SIMOX SOI wafer.

In summary, the results of the characterization task show that the crystallographic and electrical properties of the GaAs on SOI wafers are comparable to those of GaAs grown on bulk Si. From a device fabrication standpoint, the wafers show very good flatness after GaAs growth and a excellent doping profiles. These data clearly demonstrate the feasibility to grow device quality GaAs on SOI wafers.

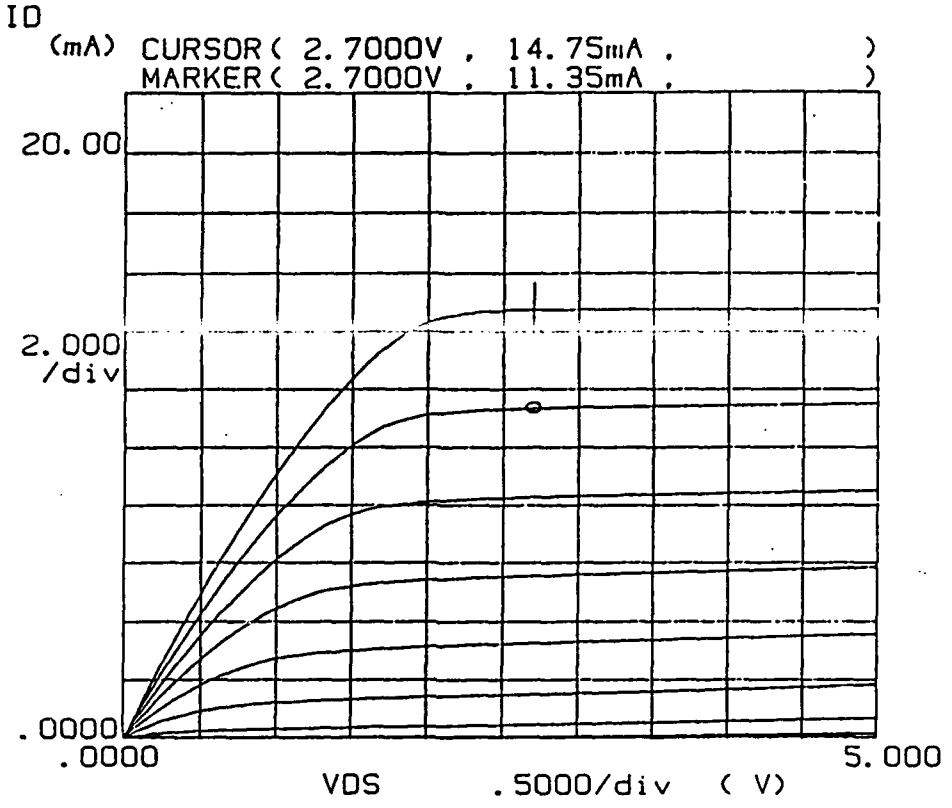
2.4 FET Fabrication and Test

The epitaxial FET wafer whose profile is shown in Figure 7 was used for the fabrication of test FET devices at Kopin. A special fabrication sequence was used in order to demonstrate the ability to achieve complete electrical isolation of individual transistors using the buried oxide layer. This is believed to be the first demonstration of an active device fabricated in GaAs on SOI.

In the process sequence, ohmic contacts were formed using Au/Ge/Ni metallization furnace alloyed at 450 °C. Aluminum was used as the gate metallization. The gate length and width for the test devices was 3 and 100 microns, respectively, and the source to drain spacing was 9 microns. This structure does not lend itself to high performance but is useful for parametric testing. Discrete FET isolation was achieved by etching away the GaAs layer between the discrete FETs and self-stopping on the Si layer. The Si layer was subsequently etched using a CF_4/O_2 plasma which self-stopped at the buried oxide surface. This process resulted in discrete GaAs on SOI FETs that were physically isolated by the oxide layer from adjacent devices and the Si substrate.

Figure 8 shows the current-voltage characteristics of such a transistor. The transconductance for this device is 68 mS/mm and compares well with the 50 to 100 values typically obtained for test devices fabricated using this geometry on both bulk GaAs and GaAs on bulk Si substrates. Measurements of current versus voltage between adjacent devices and a device and the substrate backside, shown in Figures 9 and 10, respectively, indicate that complete isolation of the devices is achieved. The device-to-device leakage, measured between the source and drain contacts of adjacent FETs, is less that 50 pA at 10 volts bias for a pad spacing of 200 microns. This is at the limits of the measurement system, and it is a very important finding.

These results clearly show that active majority carrier devices can be fabricated in GaAs on SOI wafers and that the buried oxide can be employed to achieve complete dc isolation.



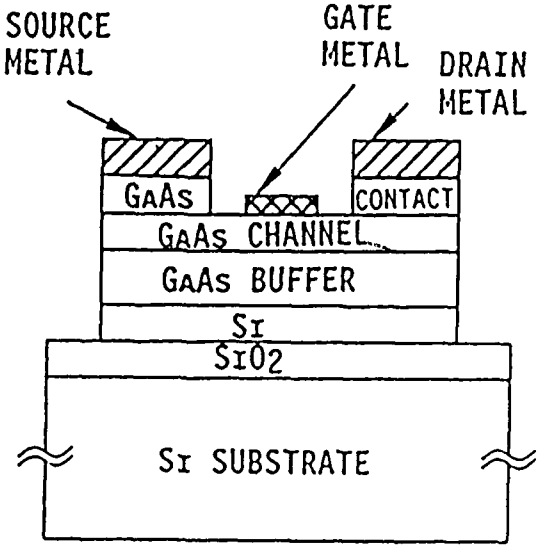
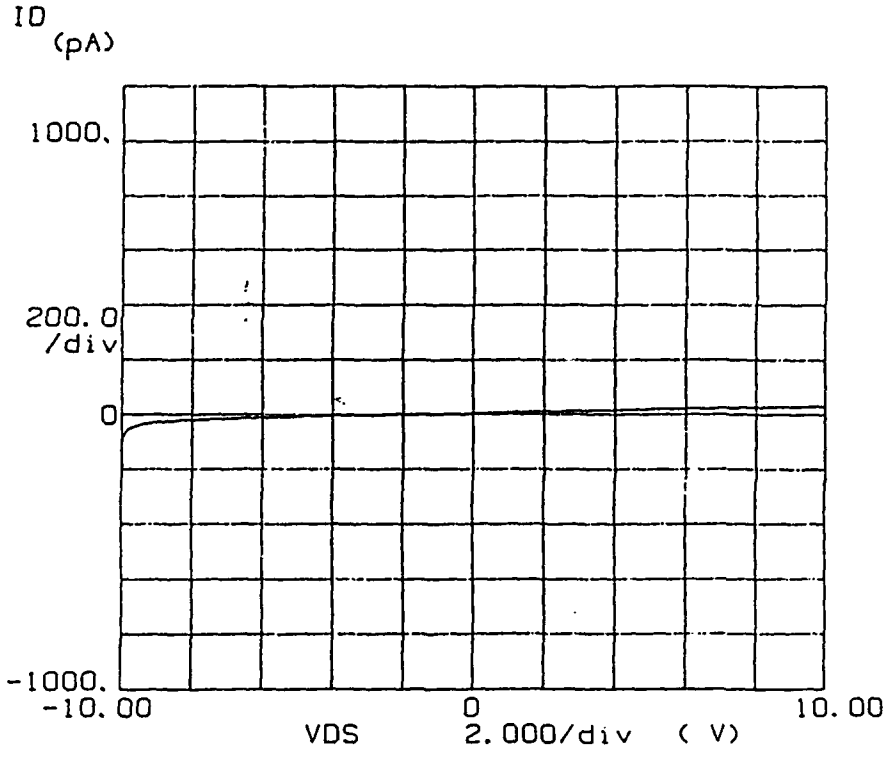


Figure 8: Current-voltage characteristics of GaAs on SOI FET.



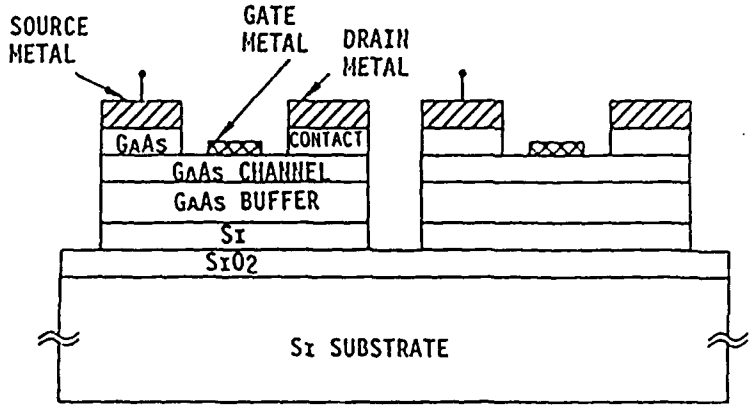
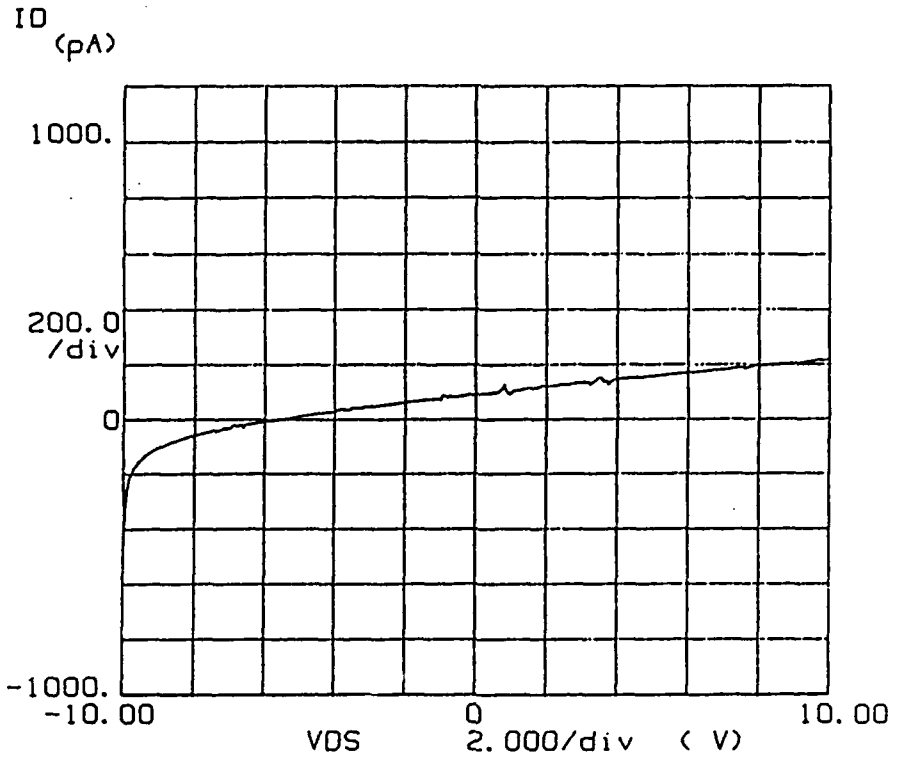


Figure 9: Current versus bias voltage measured between source and drain of adjacent isolated transistors.



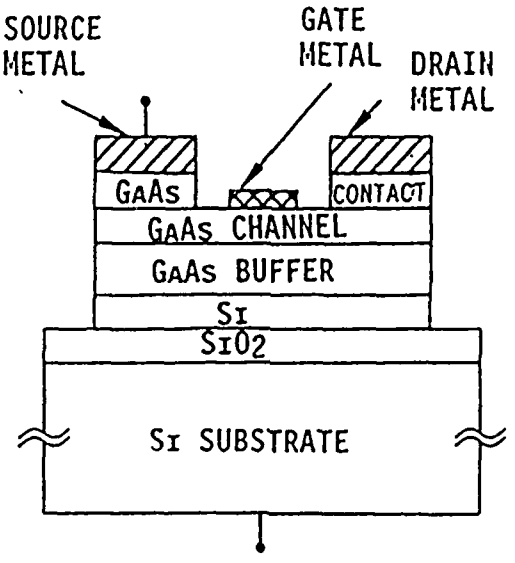


Figure 10: Current versus bias voltage measured between transistor source contact and substrate backside.

2.5 Identification of Problem Areas

The project has demonstrated the feasibility to obtain high quality GaAs on SOI wafers using the OMCVD process using both ISE and SIMOX substrates. As expected, growth on a Si surface slightly misoriented from the (100) resulted in the best morphology and suppression of antiphase domain formation using a standard epitaxy process. The residual defect structure of the GaAs layer grown on the ISE wafer indicates a suppression of dislocation propagation into the GaAs layer, an important point. Thus the areas for additional work include:

1. Modification of the OMCVD growth technique to be more compatible with growth near the (100) pole.

2. Further investigation of the nature of seeding in the ISE process to allow for the formation of a Si layer with a misorientation deviating slightly from the (100).

3. Additional investigation of the character of the dislocations in the GaAs grown on ISE and SIMOX.

4. Further investigation of the optimal GaAs on SOI structure for electronic device fabrication and operation.

5. Further studies of FETs and other devices using the GaAs-on-Insulator structure.

6. Selective growth of GaAs on SOI.

7. Monolithic integration of GaAs and Si electronic devices.

These areas constitute the body of the work that should be included in a Phase II program.

3.0 Summary

During this Phase I program we have evaluated the feasibility of the heteroepitaxy of high quality GaAs on SOI substrates by the OMCVD process. The motivation for this is the potential to obtain large area GaAs wafers with improved radiation hardness. In addition, the SOI wafer can eventually be employed for the monolithic integration of radiation hardened Si and GaAs components.

The program has been extremely successful in that epitaxial GaAs has been grown on both ISE and SIMOX wafers. The use of SIMOX provided an efficient means to obtain SOI wafers with the proper Si surface orientation compatible with a standard GaAs on

Si growth technology. However, although misoriented ISE layers were not obtained in this Phase I study, the GaAs grown on ISE shows an improved defect structure while the high quality oxide/silicon interface characteristic of the ISE process is maintained. An excellent surface morphology was obtained for GaAs grown on the misoriented SIMOX wafer. The morphology of epitaxial GaAs grown on ISE wafers showed features characteristic of growth on singular (100) surfaces.

Using SIMOX substrates, GaAs on SOI FET profiles were achieved by doping during the epitaxy process. The C-V doping profile of this structure showed flat doping plateaus for both the channel and contact levels, excellent abruptness, and a residual carrier concentration of less than 10^{14} cm^{-3}. Test FETs were processed in this wafer using etching to the buried oxide layer to achieve discrete device isolation. The FETs showed good performance with a measured transconductance of 68 mS/mm for a 3 micron gate length device with a 9 micron source-drain spacing. This is apparently the first successful demonstration of a device fabricated in GaAs on SOI, and in addition, the complete isolation achieved on this new GaAs-on-Insulator structure should have important advantages in resolving backgating and sidegating effects observed in devices fabricated in bulk GaAs wafers.

The results of this research program, in additional to demonstrating the feasibility of the heteroepitaxy of high quality GaAs on SOI wafers by OMCVD, show that the quality of the GaAs epilayer is sufficient to fabricate active majority carrier devices. It also demonstrates that the growth process can be used for the formation of active device profiles layers by doping and compositional modulation. These results provide a strong basis for continuation of the project at a Phase II contract level where monolithic integration of GaAs and Si devices can be demonstrated in GaAs on SOI wafers.

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